REMARKS

Rejection of the Claims under 35 U.S.C. §112

The examiner rejected claims 2-17, 19-24, and 26-31 under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

With respect to claims 2, 19, and 26 the examiner stated that the preamble is a method for coding test pattern but there is no step for coding test pattern in the body of the claim. Applicants submit that the body of the claims comprise several method steps which altogether are combined to achieve the claimed method invention. Hence, a claimed method invention cannot itself be a single step among several steps, in the present application. To state this another way, the preambles of the independent claims reflect the title of the invention and the recited method steps are the parts of the invention. Applicants believe that it would be vague and unclear in the present application to recite, in the body of the claim, that a single step is the same as the overall invention method.

With respect to claims 3, 20, and 27, the examiner stated that "said means" does not have clear antecedent basis. Applicants have amended claim 3 to read "said computer program", which has clear antecedent basis in claim 1, lines 5-6. Applicants have also amended claims 20 and 27 to read "said method" which has clear antecedent basis in claim 19, lines 7-8, and claim 26, lines 8-9, respectively.

With respect to claim 10, the examiner stated that "the user" does not have clear antecedent basis. Applicants have amended claim 10, line 9, to read "a user", thereby removing the ambiguous antecedent reference.

Objections to the claims

(1) The examiner stated that the claimed method step of "specifying a logic model" should be shown in a flow chart or flow diagram. Applicants have replaced the step of "specifying a logic model" with "generating a logic model" to more closely correlate with the language used in the specification. This is supported at least in paragraph [0012] (and also in paragraph [0049] below) which states:

> The method in particular includes the generation of an executable logic model representation of the physical BIT-HW . . .

Furthermore, paragraph [0049] describes the flow diagram of Fig. 1 as follows:

> It generates from IC design data (block 110) a particular data file, called BIT-CODE (block 118). The BIT-CODE (block 118) can be considered as a logic model representation of the physical BIT-HW design.

Hence, applicants believe that the claimed step of "generating a logic model" is adequately shown in the flow diagram of Fig. 1 at least at block 118 and its associated description, and respectfully request that the examiner remove the objection to the method step of "generating a logic model".

(2) The examiner stated that the claimed method step of "specifying test vectors" should be shown in a flow chart or flow diagram. Paragraph [0046] states, with reference to Fig. 1:

> The ATPG system (block 112) generates deterministic test vectors from IC design data (block 110). It should be noted that the resulting volume of test vectors (block 114) is extremely high for large ICs.

Hence, applicants believe that the claimed step of "specifying test vectors" is adequately shown in the flow diagram of Fig. 1 at least at blocks 110, 112, and 114, and their associated description, and respectfully request that the examiner remove the objection to the method step of "specifying test vectors".

(3) The examiner stated that the claimed method step of "providing the compressed test vectors" should be shown in a flow chart or flow diagram. Paragraphs [0047] and [0048] state, with reference to Fig. 1:

> The flow on the right hand side includes a BIT-HW configurator (block 116), a storage unit for keeping BIT-Code (block 118), an LFSR-Coding Unit (block 120) and a storage unit for keeping compressed LFSR-Code (block 122). This flow refers to the LFSR-Coding procedure as introduced by this invention.
>
> The outputs are compressed test vectors (LFSR-Code, block 122) to be stored at ATE (not shown in Fig. 1). The decompression is done on chip by a suitable BIT-HW as described further below.

Hence, applicants believe that the claimed step of "providing the compressed test vectors" is adequately shown in the flow diagram of Fig. 1 at least at block 122 and its associated description, and respectfully request that the examiner remove the objection to the method step of "providing the compressed test vectors".

(4) The examiner stated that the claimed method step of "specifying a function operator" should be shown in a flow chart or flow diagram. Applicants have replaced the step of "specifying a function operator" with "building a function operator"

to more closely correlate with the language used in the specification. This is supported at least in paragraph [0069] which states, with reference to Fig. 6:

> Fig. 6 illustrates a method for Building LFSR Generator Code 610. In particularly, this figure corresponds to the sample LFSR shown in Fig. 5 but here in terms of linear algebra. On the right hand side, the so-called function operator B (matrix 612) represents an LFSR. The method for building B in form of a binary matrix 612 is explained with reference to Fig. 4.

Hence, applicants believe that the claimed step of "building a function operator" is adequately shown in the flow diagram of Fig. 6 at least at matrix 612 and its associated description, and respectfully request that the examiner remove the objection to the method step of "building a function operator".

(5) The examiner stated that the claimed method step of "generating an LFSR generator code" should be shown in a flow chart or flow diagram. Paragraphs [0069] through [0076] describe the method of "generating an LFSR generator code" with reference to Fig. 6, element 610. Clearly, Fig. 6 is an adequate flow chart showing initial and resulting states of matrices and an implementation step of the present invention. Paragraph [0069] has already been excerpted in the preceding section.

Hence, applicants believe that the claimed step of "building a function operator" is adequately shown in the flow diagram of Fig. 6 at least at element 610 and its associated description, and respectfully request that the examiner remove the objection to the method step of "generating an LFSR generator code".

(6) The examiner stated that the claimed method step of "generating state-functions" should be shown in a flow chart or flow diagram. Applicants have

replaced the step of "generating state-functions" with "building state-functions by" to more closely correlate with the language used in the specification. This is supported at least in paragraphs [0080] through [0086] which describe the building of state functions with reference to Fig. 7, e.g., elements 708 and 712. Clearly, Fig. 7 is an adequate flow chart showing initial and resulting states of matrix operations linked by arrows, thereby illustrating an implementation step of the present invention.

Hence, applicants believe that the claimed step of "building state-functions" is adequately shown in the flow diagram of Fig. 7 at least at state-functions 708 and 712 and their associated description, and respectfully request that the examiner remove the objection to the method step of "building state-functions."

CONCLUSION

Applicants have properly accommodated each of the examiner's grounds for rejecting the present claims and for objecting to the present claims, as explained above. Applicants submit that the present application is now in condition for allowance.

If the Examiner has any questions or believes further discussion will aid examination and advance prosecution of the application, a telephone call to the undersigned is invited.

Respectfully submitted,

October 24, 2006

___/Eugene I. Shkurko/____
Eugene I. Shkurko
Reg. No. 36,678

IBM
Intellectual Property Law
2455 South Road, P386
Poughkeepsie, NY 12601
Phone: 845-433-1163
Fax: 845-432-9786